CLAIMS

What is claimed is:

1. A laser driver circuit comprising:

an input stage to receive an input signal;

a limiting amplifier to generate a pulse data output signal in response to the input signal, the pulse data output signal comprising a duty cycle;

an output stage to modulate an output current signal based upon the pulse data output signal; and

a duty cycle control circuit to control the duty cycle of the pulse data output signal based, at least in part, on an approximation of an average power of the pulse data output signal.

2. The laser driver circuit of claim 1, wherein the input signal comprises a bi-level signal.

3. The laser driver circuit of claim 1, wherein the input stage generates a differential signal on first and second terminals coupled to the limiting amplifier, and wherein the duty cycle control circuit comprises a current steering circuit to apply an offset current to at least one of the first and second terminals in response to the approximation of the average power of the pulse data output signal.

4. The laser driver circuit of claim 1, wherein the duty cycle control circuit further comprises a potentiometer settable to adjust the duty cycle of the pulse data output signal.

5. The laser driver circuit of claim 4, wherein the duty cycle control circuit further comprises a differential amplifier to generate a differential voltage on first and second terminals in response to the pulse data output signal, and wherein the potentiometer is coupled to the differential amplifier to determine a resistance between a voltage source and at least one of the first and second terminals to affect the differential voltage.

6. The laser driver circuit of claim 5, wherein the potentiometer is settable to allocate a resistance coupled between the voltage source and each of the first and second terminals.

7. A method comprising:

generating a pulse data output signal in response to an input signal, the pulse data output signal comprising a duty cycle;

controlling the duty cycle of the pulse data output signal based, at least in part, upon an approximation of the average power of the pulse data output signal.

8. The method of claim 7, wherein the method further comprises:

generating a differential signal on first and second terminals in response to the input signal; and

applying an offset current to at least one of the first and second terminals in response to the approximation of the average power of the pulse data output signal.

9. The method of claim 7, wherein the method further comprises setting a potentiometer to adjust the duty cycle of the pulse data output signal.

10. The method of claim 9, wherein the method further comprises:

generating a differential voltage on first and second terminals in response to the pulse data output signal; and

setting the potentiometer to determine a resistance between a voltage source and at least one of the first and second terminals to affect the differential voltage.

11. The method of claim 10, wherein the method further comprises setting the potentiometer to allocate a resistance coupled between the voltage source and each of the first and second terminals.

12. A system comprising:

a serializer to provide a serial data signal in response to a parallel data signal;

a laser device adapted to be coupled to an optical transmission medium to transmit an optical signal in the optical transmission medium in response to a current signal; and

a laser driver circuit comprising:

an input stage to receive an input signal;

a limiting amplifier to generate a pulse data output signal in response to the input signal, the pulse data output signal comprising a duty cycle;

an output stage to modulate the current signal based upon the pulse data output signal; and

a duty cycle adjustment circuit to adjust the duty cycle of the pulse data output signal based, at least in part, on an approximation of an average power of the pulse data output signal.

13. The system of claim 12, the system further comprising a SONET framer to provide the parallel data signal.

14. The system of claim 13, wherein the system further comprises a switch fabric coupled to the SONET framer.

15. The system of claim 13, the system further comprising an Ethernet MAC to provide the parallel data signal at a media independent interface.

16. The system of claim 15, wherein the system further comprises a multiplexed data bus coupled to the Ethernet MAC.

17. The system of claim 15, wherein the system further comprises a switch fabric coupled to the Ethernet MAC.